AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method comprising:

writing an initial value to at least one address within a memory image residing in dynamic random access memory, said memory image being generated as a result of performing a state save operation;

adjusting a control value for a control register as a function of a control register mask to generate a masked control value;

storing said masked control value in the control register, wherein a status of at least one reserved bit of the control register is to indicate whether a processor, which is to perform ~~the~~ a state save operation, is capable of performing of performing a ~~select~~ function uniquely corresponding to the reserved bit.

2. (Previously Cancelled)

3. (Previously presented) The method of claim 1 further comprising executing ~~a~~ the state save operation.

4. (Previously Presented) The method of claim 3 further comprising comparing a saved value to said initial value, said saved value being stored within said memory image as a result of said execution of said state save operation.

5. (Previously Presented) The method of claim 4 wherein said control register mask is set to a default value if said saved value is equal to said initial value.

6. (Previously Presented) The method of claim 5 wherein said control register mask is set to said saved value if said saved value is not equal to said initial value.

7. (Previously Cancelled)

8. (Previously Presented) The method of claim 6 wherein said state save operation is an FXSAVE instruction, said FXSAVE instruction having an associated target address.

9. (Previously Presented) The method of claim 8 wherein said target address is an address within said memory image.

10. (Currently Amended) A machine-readable medium having stored thereon a set of instructions said set of instructions, which when executed by a processor, cause said processor to perform a method comprising:

writing an initial value to at least one address within a memory image residing in dynamic random access memory, said memory image being generated as a result of performing a state save operation;

adjusting a control value for a control register as a function of a control register mask to generate a masked control value;

storing said masked control value into the control register, which is to perform a ~~the~~ state save operation, is capable of performing of performing a ~~select~~ function uniquely corresponding to the reserved bit.

11. (Cancelled)

12. (Previously Presented) The computer-readable medium of claim 10 further comprising executing the state save operation.

13. (Previously Presented) The computer-readable medium of claim 12 further comprising comparing a saved value to said initial value, said saved value being stored within said memory image as a result of said execution of said state save operation.

14. (Previously Presented) The computer-readable medium of claim 13 wherein said control register mask is set to a default value if said saved value is equal to said initial value.

15. (Previously Presented) The computer-readable medium of claim 14 wherein said control register mask is set to said saved value if said saved value is not equal to said initializing value.

16. (Cancelled)

17. (Previously Presented) The computer-readable medium of claim 15 wherein said state save operation is an FXSAVE instruction, said FXSAVE instruction having an associated target address.

18. (Original) The computer-readable medium of claim 17 wherein said target address is an address within said memory image.

19. (Currently Amended) An apparatus comprising:

a control register comprising a plurality of control bits, each to uniquely indicate ~~corresponding to~~ a ~~plurality of~~ functions that a processor is capable of performing;

a masking mechanism to generate a control register mask by setting inactive one or more bits of a control value prior to storage of said one or more bits in the control register, wherein the masking mechanism includes a mask storage area within dynamic random access memory to store state information corresponding to state information stored in the control register, said mask storage area having been generated as a result of performing a state save operation.

20. (Cancelled)

21. (Previously Presented) The apparatus of claim 19 wherein said mask storage area may be accessed by performing a state saving operation which saves said mask value to a memory location.

22. (Original) The apparatus of claim 21 wherein said state saving operation is an FXSAVE instruction.

23. (Original) The apparatus of claim 19 wherein said masking mechanism is a hardware masking mechanism.

24. (Previously Presented) The apparatus of claim 19 wherein said masking mechanism comprises:

a sequence of instructions to adjust a control value by saving state information including a control register value to a memory and adjusting said control register value based on a readable mask value read from the processor before restoring the state information;

execution hardware to execute the sequence of instructions.

25. (Currently Amended) A processor comprising:

a decode unit;

at least one of a plurality of registers, said at least one of a plurality of registers comprising a plurality of control bits, each uniquely to indicate ~~corresponding to~~ a ~~plurality of~~ functions that the processor is capable of performing;

a masking mechanism to generate a control register mask by setting ~~to set~~ inactive one or more bits of a control value prior to storage of said one or more bits in the control register, wherein the masking mechanism includes a mask storage area within dynamic random access memory to store state information corresponding to state

information stored in the at least one of the plurality of register, said mask storage area having been generated as a result of performing an instruction;

an execution unit;

an internal bus, said decoder unit, said at least one plurality of registers, said at least one execution unit being coupled by said internal bus.

26. (Previously Presented) The processor of claim 25, wherein, in response to said execution unit executing the instruction, said plurality of bits are written to the mask storage area.

27. (Original) The processor of claim 26 wherein said instruction is an FXSAVE instruction.

28. (Original) The processor of claim 27 wherein said at least one of a plurality of registers is an MXCSR register.

29. (Previously Presented) The processor of claim 28 wherein said mask storage area is an MXCSR_MASK field.